

REMARKS

Applicant respectfully requests reconsideration and allowance of the subject application. Claims 1-9 are pending, of which claims 1, 3, and 6 have been amended. The amendments made to claims 3 and 6 are purely to correct typographical errors noted by the Applicant, and not to overcome prior art.

Claim 1 has been amended in the interest of clarity. Claim 1, as amended, is in condition for allowance. All remaining claims depend from claim 1 and thus are also in condition for allowance.

35 U.S.C. §102 Claim Rejections

Claim 1 is rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No.6,327,463 B1, to Welland et al. (hereinafter "Welland"). With respect to claim 1 as amended, Applicant respectfully traverses the rejection.

The subject invention

The subject invention is a phase-locked loop circuit having a voltage-controlled oscillator, wherein the voltage-controlled oscillator comprises a resonator circuit. The resonator circuit drives the oscillator at an oscillator output frequency that is an integer multiple of the resonator frequency. The resonator frequency is coupled to the frequency control means of the phase-locked loop. In this manner, the phase-locked loop need only handle a fraction of the full RF output frequency of the oscillator. Thus, the need for additional frequency dividers or multipliers as found in the prior art is eliminated.

Welland

Welland teaches a method and apparatus for synthesizing high-frequency signals to limit phase noise and other signal impurities. Welland uses a phase-locked loop frequency synthesizer with a variable capacitance voltage-controlled oscillator that includes both discretely and continuously variable capacitance. The variable capacitance is used in conjunction with an LC tank oscillator circuit to drive the voltage-controlled oscillator. The discretely variable capacitance provides a coarse tuning adjustment to compensate for capacitor and inductor tolerances when adjusting the output frequency. The continuously variable capacitance provides a fine tuning adjustment to the output frequency.

The output from the voltage-controlled oscillator is fed to a frequency divider circuit (divide by N counter 214 of Fig. 2). The resulting divided signal is received by a phase detector within the phase-locked loop (202 of Fig. 2), and the divided signal is used by phase-locked loop to control its output frequency to a loop filter and then to the voltage-controlled oscillator.

Specific Rejections under 35 U.S.C. § 102

The Examiner has rejected claim 1 as being anticipated by Welland.

Specifically, the Examiner states that “Welland et al. discloses a phase-locked loop circuit comprising: a voltage controlled oscillator (Fig. 2, 212) which includes at least one resonator circuit (Fig. 3 and Fig. 4) for driving the oscillator; a phase-locked loop including frequency control means (ABSTRACT) for controlling the output frequency of said oscillator, such that during operation said resonator circuit runs at a resonator frequency to drive said oscillator output frequency which is an integer multiple of the resonator frequency (col. 7, lines 45-67, col. 8, lines 1-60); wherein the resonator frequency is coupled to the frequency control means of the phase-locked loop, in that

the resonator circuit includes at least one adjustable component to control the resonator frequency and that in the phase locked loop frequency control means are coupled to the resonator circuit for controlling the resonator frequency (Fig. 4 and 5, column, lines 17-65; column 9, lines 33+..)." With respect to this rejection as applied to amended claim 1, Applicant respectfully traverses.

In order for a rejection under 35 U.S.C. §102 to be proper, each and every element of a claim must be found in the cited reference. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987) M.P.E.P. §2131.

Claim 1, as amended, recites:

[a] Phase-locked loop circuit comprising:

a voltage-controlled oscillator which includes at least one resonator circuit for driving the oscillator;

a phase-locked loop including frequency control means for controlling the output frequency of said oscillator, such that during operation said resonator circuit runs at a resonator frequency to drive said oscillator at an oscillator output frequency which is an integer multiple greater than one of the resonator frequency;

wherein the resonator frequency is coupled to the frequency control means of the phase-locked loop, wherein the resonator circuit includes at least one adjustable component to control the resonator frequency.

Welland fails to disclose each of the elements of claim 1. First, Applicant submits that Welland fails to disclose the use of a resonator circuit for driving the oscillator, as claimed in claim 1. Welland uses an LC tank oscillator having an external inductor to drive the voltage controlled oscillator.

Even if, *assuming arguendo*, that the LC tank circuit used in Welland can be equated to a resonator as claimed, Welland still fails to disclose the invention as claimed in claim 1.

One aspect of the claimed invention is to allow the phase-locked loop to operate with a voltage controlled oscillator having an output frequency higher than that which can be handled by the phase-locked loop frequency control means without requiring additional frequency divider circuitry in the feedback loop. Welland does not address this concern. The configuration of Welland is in accordance with the prior art as shown in Fig. 1 of the current application. In Welland, the output of the voltage controlled oscillator is subjected to a frequency divider circuit (214 of Fig. 2), and the output of this frequency divider circuit is coupled to the frequency control means of the phase-locked loop. This configuration is claimed in claim 1, and Welland fails to anticipate these elements.

Claim 1 recites a phase-locked loop including frequency control means for controlling the output frequency of said oscillator, such that during operation the resonator circuit runs at a resonator frequency to drive the oscillator at an oscillator output frequency which is an integer multiple greater than one of the resonator frequency. Claim 1 also recites that the resonator frequency is coupled to the frequency control means of the phase-locked loop. By using the resonator frequency instead of the output frequency of the voltage-controlled oscillator, no additional circuitry (in the form of a frequency divider or multiplier) is required.

Welland does not disclose using a resonator frequency to drive the voltage-controlled oscillator at an oscillator output frequency which is an integer multiple greater than one of the resonator frequency, as recited in claim 1. In Welland, the actual output of the voltage-controlled oscillator is supplied to a frequency divider circuit. The output signal of the voltage-controlled oscillator is not an integer multiple

greater than one of a resonator frequency. There is only one output in Welland. Clearly, since two outputs signal from the voltage-controlled oscillator are not present in Welland, a resonator frequency to drive said oscillator at an oscillator output frequency which is an integer multiple greater than one of the resonator frequency, as claimed in claim 1, is not taught. Thus, this feature is not anticipated by Welland.

Furthermore, Welland does not anticipate the element of claim 1 wherein the resonator frequency is coupled to the frequency control means of the phase-locked loop. In Welland, the output of the LC tank circuit is not coupled to the frequency control means of the phase-locked loop. The configuration of Welland is such that the output of the voltage controlled oscillator is coupled to a frequency divider circuit (divide by N counter 214 of Fig. 2 of Welland). Because the output of the LC tank circuit and the output of the voltage-controlled oscillator are the same (i.e., there is only one output in Welland), and by nature the frequency of this output is higher than that which can be accepted by the phase-locked loop, a divider circuit is necessary before coupling to the frequency control means of the phase-locked loop. The configuration taught in Welland is shown as prior art in Figure 1 of the Applicant's specification.

Welland does not teach the use of a resonator circuit, does not teach using a resonator frequency to drive the voltage-controlled oscillator at an oscillator output frequency which is an integer multiple greater than one of the resonator frequency, and does not teach coupling the resonator output to the frequency control means of the phase-locked loop. All of these elements are claimed in claim 1. Thus, clearly Welland does not anticipate claim 1. Claim 1, as amended, is patentable over Welland and in condition for allowance.

All of the remaining claims depend from claim 1. As a result, claims 2-9 are also in condition for allowance.

35 U.S.C. §103 Rejections

The Examiner has rejected claims 2-9 under 35 U.S.C. 103(a) as being unpatentable over Welland in view of U.S. Patent No. 6,268,778 B1 issued to Mucke et al. Claims 2-9, however, are all dependent upon claim 1. Mucke has been cited for reasons unrelated to the missing elements of claim 1, and therefore does not provide the necessary teaching lacking from Welland. Thus, claims 2-9 are in condition for allowance for the reasons as set forth above, and the rejections of claims 2-9 under 35 U.S.C. 103(a) are moot.

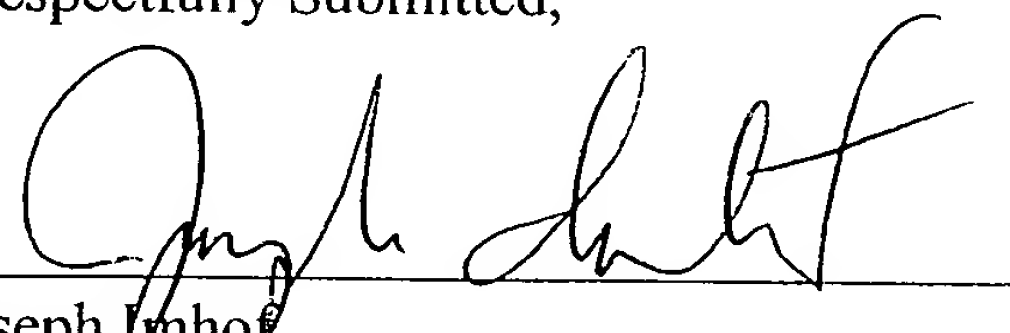
Conclusion

Pending Claims 1-9 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. If any issues remain that preclude issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Dated: 6-4-2003

By: _____


Joseph Imhof
Reg. No. 41,863
(215) 923-4466